Bilingual Semiconductor Technical Lead

募集職種

人材紹介会社
IZUMI NETWORK

求人ID
1615943

業種
電気・電子・半導体

雇用形態
正社員

勤務地
東京都 23区

給与
900万円 ~ 1600万円

更新日
2026年11月16日 01:00

応募必要条件

職務経験
6年以上

キャリアレベル
中途経験者レベル

英語レベル
ビジネス会話レベル

日本語レベル
ビジネス会話レベル

最終学歴
大学卒： 学士号

現在のビザ
日本での就労許可が必要です

募集要項

Position Summary
We are seeking an experienced **Bilingual Semiconductor Technical Lead** to support advanced SoC implementation projects for Synopsys Japan.

The successful candidate will act as the onsite technical lead, working directly with customers in Japan while coordinating global engineering teams. This position requires strong expertise across the RTL-to-GDSII implementation flow, with particular focus on synthesis, timing closure, signoff, and tapeout activities.
This role combines technical leadership, customer engagement, and project execution responsibilities.

Key Responsibilities

- Act as the primary technical lead for customer-facing projects.
- Lead technical discussions with customers and internal engineering teams.
- Coordinate onsite and offshore engineering resources.
- Drive RTL-to-GDSII implementation activities.
- Support synthesis, timing closure, signoff, and tapeout execution.
- Drive Performance, Power, and Area (PPA) optimization.
- Identify technical risks and implementation bottlenecks.
- Collaborate closely with RTL, Physical Design, DFT, Verification, and EDA teams.
- Track project milestones and support successful project delivery.

スキル・資格

Required Skills & Experience

- 8+ years of semiconductor design and implementation experience.
- Strong understanding of the complete RTL-to-GDSII implementation flow.

Hands-on experience in:

- Synthesis
- Static Timing Analysis (STA)
- Timing Closure
- Signoff Methodology
- Tapeout Activities

Experience with:

- Design Compiler
- Fusion Compiler
- PrimeTime
- SDC Constraint Development
- Logic Equivalence Check (LEC)

Strong understanding of how RTL decisions impact:

- Timing
- Power
- Congestion
- Testability
- Physical Implementation

1. Experience leading technical teams or project delivery activities.
2. Customer-facing experience is highly preferred.

Preferred Skills

- ICC2
- StarRC
- VC SpyGlass
- Floorplanning
- Place & Route (PnR)
- Clock Tree Synthesis (CTS)
- DRC/LVS
- Low Power Design
- Advanced-node implementation experience

Language Requirements:
Japanese: Business Level or above (**Mandatory**)
English: Business Level (**Mandatory**)

Preferred Background:
Candidates from the following companies or similar environments are highly preferred:

- Synopsys
- Cadence
- Socionext
- Renesas
- TSMC
- Rapidus Ecosystem
- Semiconductor Design Service Companies
- ASIC Design Houses

会社説明