



## PR/160721 | IP Design Engineer (RTL & Synthesis | FPGA & High-Speed Interfaces)

### 募集職種

#### 人材紹介会社

ジェイエイシーリクルートメントマレーシア

#### 求人ID

1599405

#### 業種

電気・電子・半導体

#### 雇用形態

正社員

#### 勤務地

マレーシア

#### 給与

経験考慮の上、応相談

#### 更新日

2026年06月26日 11:15

### 応募必要条件

#### 職務経験

6年以上

#### キャリアレベル

中途経験者レベル

#### 英語レベル

流暢

#### 日本語レベル

無し

#### 最終学歴

短大卒：準学士号

#### 現在のビザ

日本での就労許可は必要ありません

### 募集要項

Join a fast-growing semiconductor design organization developing cutting-edge FPGA IP solutions for next-generation networking and high-performance systems.

This role offers the opportunity to work across the full IP development lifecycle—from architecture definition to RTL implementation and silicon validation—while collaborating with global engineering teams. If you enjoy building scalable, high-performance designs and working on advanced protocols, this is a strong platform for career growth.

#### Key Responsibilities

- Understand FPGA architectures, application use cases, and protocol standards
- Define system architecture and develop algorithm models using C/C++ or MATLAB
- Develop high-quality RTL code using Verilog/VHDL
- Build verification environments using SystemVerilog

- Perform simulation, debugging, and validation to ensure design robustness
- Deliver complete IP solutions from concept to implementation  
Package IP using EDA tools and develop user-friendly interfaces (GUI)
- Ensure IP quality through comprehensive testing and validation
- Provide technical training and guidance to FAEs
- Support customer integration, debugging, and deployment activities
- Gather feedback from field teams and customers to enhance IP performance and features
- Contribute to ongoing improvements and next-generation IP development

**Key Requirements**

- 5+ years of experience in FPGA / RTL / digital design
- Bachelor's degree or above in Electronics, Microelectronics, Communications, or Computer Science
- Strong proficiency in Verilog/VHDL
- Hands-on experience with FPGA tools: Vivado, ISE, or Quartus
- Experience with simulation tools: Synopsys VCS, Verdi, Cadence, or ModelSim
- Solid understanding of digital front-end design and timing closure
- Knowledge of FPGA development methodologies (top-down / bottom-up)
- Familiarity with DFT concepts and performance optimization
- Strong problem-solving mindset with innovative thinking
- Good communication skills and ability to collaborate across teams
- Ability to manage tasks and contribute in a fast-paced environment

**Nice-to-Have (Stand Out Skills)**

- DSP / Algorithm Design
- Experience with FIR, FFT, DUC/DDC, CFR
- Familiarity with Xilinx System Generator
- High-Speed Interfaces
- Experience with protocols such as PCIe, NVMe, SATA, SRIO, or AURORA

**Notice:** By submitting an application for this position, you acknowledge and consent to the disclosure of your personal information to the Privacy Policy and Terms and Conditions, for the purpose of recruitment and candidate evaluation.

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会社説明