



マレーシアの求人なら
JAC Recruitment Malaysia

PR/160720 | Lead IO Mixed-Signal Design Engineer (High-Speed Connectivity | Advanced Nodes)

募集職種

人材紹介会社
ジェイエイシーリクルートメントマレーシア

求人ID
1599404

業種
電気・電子・半導体

雇用形態
正社員

勤務地
マレーシア

給与
経験考慮の上、応相談

更新日
2026年08月07日 19:00

応募必要条件

職務経験
6年以上

キャリアレベル
中途経験者レベル

英語レベル
流暢

日本語レベル
無し

最終学歴
短大卒：準学士号

現在のビザ
日本での就労許可は必要ありません

募集要項

Join a fast-growing semiconductor design organization at the forefront of high-speed interface and connectivity solutions. This is an exciting opportunity to lead cutting-edge mixed-signal IO design for next-generation applications, working with advanced process technologies and a highly collaborative global team. If you are passionate about solving complex analog challenges, driving innovation, and leading technical teams, this role offers strong visibility, ownership, and career progression.

Key Responsibilities

- Lead and mentor a team of design engineers, providing technical direction and driving project execution
- Act as a key decision-maker for design methodologies and technical strategies
- Define chip-level architecture and module specifications for high-speed IO designs
- Translate system requirements into robust mixed-signal circuit solutions

- Design and develop high-performance IO circuits using full-custom methodologies
- Work on advanced technology nodes, ensuring performance, scalability, and reliability
- Partner with backend, DFT, and system teams on floorplanning, modeling, and optimization
- Collaborate closely with global stakeholders to align design goals and timelines
- Drive DRC/LVS verification and ensure high-quality GDSII delivery
- Support silicon bring-up, validation, and performance tuning

Key Requirements

- 8+ years in semiconductor design (mixed-signal / IO / SoC preferred)
- Strong hands-on experience in full-custom IC design
Proficiency with EDA tools: Cadence, Virtuoso, Spectre, Hspice, AMS
- Deep understanding of analog circuit design and signal integrity
- High-speed interfaces: DDR3/4/5, LPDDR, LVDS Or experience with PLL, ADC, clocking networks
- Experience leading or mentoring engineers
- Strong communication skills with ability to work across global teams
- Mandarin proficiency is a plus
- Bachelor's degree or above in Electrical Engineering, Microelectronics, or related field

Notice: By submitting an application for this position, you acknowledge and consent to the disclosure of your personal information to the Privacy Policy and Terms and Conditions, for the purpose of recruitment and candidate evaluation.

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会社説明