



【800～2500万円】Digital Design Engineer

外資系半導体メーカーでの募集です。弱電回路設計のご経験のある方は歓迎です。

募集職種

人材紹介会社

株式会社ジェイ エイ シー リクルートメント

採用企業名

外資系半導体メーカー

求人ID

1593778

業種

電気・電子・半導体

会社の種類

外資系企業

雇用形態

正社員

勤務地

東京都 23区

給与

800万円～2500万円

勤務時間

09:00～18:00

休日・休暇

詳細は求人ご紹介時にご案内いたします。

更新日

2026年06月25日 06:00

応募必要条件

キャリアレベル

中途経験者レベル

英語レベル

ビジネス会話レベル

日本語レベル

ネイティブ

最終学歴

大学卒：学士号

現在のビザ

日本での就労許可が必要です

募集要項

【求人No NJB2381570】

- ・ Developing micro architecture specification of the logic circuit from reading and comprehending the Product Requirement Document (PRD) .
- ・ Developing the Register Transfer Level (RTL) design from the micro architecture specification using Verilog or SystemVerilog as the HDL.
- ・ Developing standalone test benches to verify the RTL behavior.
- ・ Writing and verifying SystemVerilog Assertions (SVA) for a design.

- Writing timing constraints and clock definition for synthesis and place and route tools.
 - Running industry standard synthesis tools (e.g. Genus or Design Compiler) and being able to fix timing problems if they arise.
 - Understanding various design tradeoffs including timing/area/power and knowing how to improve them.
 - Reading and understanding the Static Timing Analysis (STA) reports from an industry standard STA tool (e.g. Prime Time) .
 - Cross functional interactions and communication with various teams within SiTime including analog verification backend system and test engineering teams.
 - Post Si bring up validation and debugging.
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スキル・資格

【Qualifications Requirements】

- Master's degree in electrical engineering plus 5 years of relevant work experience in the industry.
- Excellent verbal and written communication skills in English.
- Proficient in Verilog and SystemVerilog.
- Expertise in digital logic design fundamentals such as clock divider circuits multi clock logic designs CDC FIFO FSM etc.
- Experience in designing mixed signal digital logic.
- Basic understanding of Discrete time Signal Processing theory FIR and IIR filter design.
- Solid experience in digital design flow including RTL design synthesis timing constraints and STA.
- Skilled in scripting languages Perl/Tcl/Python.

【Desired Characteristics Attributes】

- Ph.D. in electrical/computer engineering plus 3 years of relevant industry experience.
 - 2 5 years of experience in designing high precision digital arithmetic logic and Digital Signal Processing.
 - 2 5 years of experience in designing Digital Phase Locked Loops (DPLL) .
 - Experience in complex FSM design.
 - Familiarity with MATLAB Simulink or any other high level modeling tools.
 - Experience in low power digital design flow.
 - Basic understanding of the Control Theory.
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会社説明

ご紹介時にご案内いたします