



【800～2500万円】Verification Engineer

外資系半導体メーカーでの募集です。弱電回路設計のご経験のある方は歓迎です。

募集職種

人材紹介会社

株式会社ジェイ エイ シー リクルートメント

採用企業名

外資系半導体メーカー

求人ID

1593777

業種

電気・電子・半導体

会社の種類

外資系企業

雇用形態

正社員

勤務地

東京都 23区

給与

800万円～2500万円

勤務時間

09:00～18:00

休日・休暇

詳細は求人ご紹介時にご案内いたします。

更新日

2026年06月25日 06:00

応募必要条件

キャリアレベル

中途経験者レベル

英語レベル

ビジネス会話レベル

日本語レベル

ネイティブ

最終学歴

大学卒：学士号

現在のビザ

日本での就労許可が必要です

募集要項

【求人No NJB2381564】

- ・ Developing SV RNM models for both analog and mixed signal circuits
- ・ Developing verification plan from chip or block specifications
- ・ Developing UVM based verification environment (scoreboards monitors sequencers etc.)
- ・ Developing digital top verification in System Verilog
- ・ Defining and writing System Verilog Assertions (SVA)
- ・ Defining and writing functional coverages and covergroups

- Running simulations and debugging simulation results
 - Reviewing verification results for Tape out sign off
 - Communicating with stakeholders (design/test/verification) to facilitate teamwork and efficient sharing of information and exchange of ideas
-

スキル・資格

【Qualifications Requirements】

- MS (BS) degree in electrical/computer engineering or related fields with 5 (8) years of work experience doing verification in the semiconductor industry
- Good verbal and written communication skills in English
- Proficient in SystemVerilog and SystemVerilog OOP
- Fluency in utilizing scripting languages such as Perl / Python
- Proficient (through work experience) in verification using UVM
- Strong experience writing SystemVerilog Assertions (SVA)
- Understanding of Analog schematic and experience with Cadence Virtuoso
- Basic understanding of digital design using Verilog
- Ability to communicate and work effectively with geographically dispersed teams of mixed signal digital design and analog design engineers
- Ability to work independently and drive solutions to challenging problems

【Desired Qualification】

- Experience with generating functional models for analog blocks using SystemVerilog RNM Wreal (V AMS) or similar techniques
 - Experience with UVM AMS methodology
 - Solid experience with Formal Property Verification (FPV)
 - Programming experience writing OOP code in C++
 - Excellent written and verbal communication skills in English
 - Experience with performing analog mixed signal verification
 - Proven track record in working well with others in fast paced and collaborative work environment
 - Knowledge of analog design
 - Knowledge of synthesizable digital design
 - Experience working on verification of datapath designs including filters
-

会社説明

ご紹介時にご案内いたします