【800 ~ 2500万円】Analog Mixed Signal Design Engineer

外資系半導体メーカーでの募集です。 弱電回路設計のご経験のある方は歓迎です。

募集職種

人材紹介会社
株式会社ジェイ エイ シー リクルートメント

採用企業名
外資系半導体メーカー

求人ID
1593774

業種
電気・電子・半導体

会社の種類
外資系企業

雇用形態
正社員

勤務地
東京都 23区

給与
800万円 ~ 2500万円

勤務時間
09:00 ~ 18:00

休日・休暇
詳細は求人ご紹介時にご案内いたします。

更新日
2026年05月28日 16:18

応募必要条件

キャリアレベル
中途経験者レベル

英語レベル
ビジネス会話レベル

日本語レベル
ネイティブ

最終学歴
大学卒： 学士号

現在のビザ
日本での就労許可が必要です

募集要項

【求人No NJB2381318】
・Contribute to the architectural definition of the design and chip integration
・Technical leader for chip level design and verification simulations to ensure building blocks meet specifications at the schematic level and after post layout extraction while fully provisioning for DFT and DFM
・Work closely with Layout Engineers to validate proper layout using all best known methods
・Document assigned blocks and hold preliminary and final design review meetings
・Actively participate in the chip bring up evaluation and characterization with emphasis on owned blocks

・Work cross functionally with Product Characterization Test and Application Engineers on issues related to owned circuit blocks
・Coach mentor and develop junior/mid level analog designers foster cross functional collaboration.

スキル・資格

【Qualifications Requirements】
・M.S. in Electrical Engineering or related field with minimum 15 years of related experience or Ph.D. in Electrical Engineering with minimum 12 years of related experience
・Excellent academic record with published research projects prototyped and proven in silicon
・Detailed knowledge of CMOS circuits and noise analysis
・Core expertise in one of the following areas:
  ・Integer N and fractional N PLL
  ・Sigma Delta ADCs
  ・Temperature sensor
  ・Analog and digital filters
  ・Quartz or MEMS oscillator
  ・Sub threshold circuits
  ・Low noise regulator and bandgap
  ・High speed output drivers
・Ability to oversee circuit layout for critical blocks
・Knowledge of programming languages: MATLAB VerilogA
・Proficient in using Cadence analog design tools
・Good facilitation skill for project/design review meeting
・Excellent analytical problem solving written/verbal communication.
・Proven leadership and ability to collaborate across system architects digital teams layout test manufacturing

【Desired Characteristics Attributes】
・Passionate self starter with a strong commitment to flawless execution
・Excellent written and verbal communication skills required
・Ability to work well with others in a fast paced collaborative team environment

会社説明

ご紹介時にご案内いたします