【アメリカ外資系】 Senior Layout Design Engineer　※イメージセンサーの基盤をデザイン

NY証券取引所上場 35か国に展開 計測機器のグローバルメーカー

募集職種

採用企業名
アメテック株式会社

求人ID
1592911

部署名
Vision Research

業種
機械

会社の種類
外資系企業

雇用形態
正社員

勤務地
東京都 23区, 港区

給与
900万円 ~ 1000万円

更新日
2026年05月27日 14:51

応募必要条件

職務経験
3年以上

キャリアレベル
中途経験者レベル

英語レベル
ビジネス会話レベル

日本語レベル
日常会話レベル

最終学歴
大学卒： 学士号

現在のビザ
日本での就労許可が必要です

募集要項

≪Job Description & Position Highlights≫

- Responsible for the end-to-end layout design and verification of analog and mixed-signal ICs
- Collaborate with circuit designers to contribute to the design of high-performance CMOS imaging semiconductors
- Utilize tools such as Cadence Virtuoso to ensure DRC/LVS compliance and perform physical verification to achieve silicon-quality results
- A highly specialized environment where you will engage in cutting-edge semiconductor design in a global setting using English

【Job Responsibilities】
We are seeking a highly skilled Senior Analog Layout Engineer to lead the physical layout of complex analog, mixed-signal, and high-performance IC designs. This role requires deep expertise in custom layout techniques, advanced process nodes, physical verification, and close collaboration with circuit designers to deliver silicon-proven designs that meet stringent performance, reliability, and manufacturing requirements.

< Primary Responsibilities >

- Own and execute the full layout lifecycle for analog and mixed-signal IP blocks such as ADCs, DACs, PLLs, LDOs, bandgaps, amplifiers, and pixels.
- Collaborate closely with circuit design engineers to understand specifications, constraints, and performance trade-offs.
- Develop floorplans, layout strategies, and routing plans that optimize matching, noise performance, EM/IR robustness
- Perform custom layout of critical analog circuits using industry-standard EDA tools (e.g., Cadence Virtuoso).
- Ensure compliance with design rules (DRC), electrical rules (ERC), layout-vs-schematic checks (LVS), and parasitic extraction (PEX).
- Drive layout quality through guard-ringing, shielding, isolation techniques, symmetry enforcement, and dummy placements.
- Work with foundry PDKs to interpret process rules, device models, and reliability requirements (ESD, EM, latch-up).
- Generate and maintain layout documentation, checklists, and layout guidelines for internal use.
- Prepare designs for tapeout, including final checks, documentation, and coordination with the fabrication team.
- Develop and maintain scripts to automate repetitive tasks, improving efficiency and consistency in the design process.
- Participate in technical reviews with design team and customer.
- Able to work independently and collaborate with local technical lead.

< About Us >
Forza Silicon is a Business Unit in the Materials Analysis Division of AMETEK, Inc. Founded in 2001, Forza Silicon has established itself as an innovator and industry leader in the field of mixed-signal IC and CMOS imaging designs that have set the standard of the possible. Primarily through long standing customer relationships and partner referrals, Forza has grown to where today the company employs one of the industry's largest and most experienced independent CMOS imaging engineering teams. To learn more about Forza Silicon, please go to www.forzasilicon.com
AMETEK, Inc. is a leading global provider of industrial technology solutions serving a diverse set of attractive niche markets with annual sales over $7.5 billion.
AMETEK is committed to making a safer, sustainable, and more productive world a reality. We use differentiated technology solutions to solve our customers' most complex challenges. We employ 22,000 colleagues, in 35 countries, that are grounded by our core values: Ethics and Integrity, Respect for the Individual, Inclusion, Teamwork, and Social Responsibility.
AMETEK is a component of the S&P 500. Visit https://www.ametek.com/careers for more information.

勤務地
東京都港区芝大門1-1-30 芝タワー
勤務地最寄駅：都営浅草・大江戸線 / 大門駅
受動喫煙対策：屋内全面禁煙
変更の範囲：会社の定める事業所（リモートワーク含む）
転勤：無
基本的には転勤はございません。
在宅勤務・リモートワーク：相談可

勤務時間
9:00 ~ 17:30（所定労働時間：7時間30分）
休憩時間：60分
時間外労働有無：有

休日休暇
週休2日制（休日は土日祝日）
年間有給休暇：
初年度1日 ~ 10日（下限日数は、入社直後の付与日数となります）
勤続 2 年未満12日、勤続2-5年16日、勤続5年以上20日
年間休日日数124日
年末年始休日（3日）、年末年始休暇（12/29 - 1/4）、夏期休暇（3日）、年次有給休暇（初年度は入社月に応じて入社日に按分付与）

手当/福利厚生
通勤手当、健康保険、厚生年金保険、雇用保険、労災保険、退職金制度

＜各手当・制度補足＞
通勤手当：全額支給※規定に基づく
社会保険：各種社会保険完備
退職金制度：勤続3年以上

スキル・資格

【Position Requirements】

- Bachelor's or Master's degree in Electrical Engineering, Electronics Engineering, or related field.
- 4-7+ years of experience in analog or mixed-signal IC layout.
- Expert proficiency with Cadence Virtuoso or equivalent layout platforms.

***Deep understanding of:**

- Analog layout matching and common centroid techniques
- Low-noise, low-offset layout methodologies
- Parasitic-aware design and optimization
- Strong understanding of DRC, LVS, PEX flows and physical verification tools (Calibre, Assura, PVS).
- Ability to work in a fast-paced, collaborative environment with designers, CAD engineers, and verification teams.
- Excellent communication and documentation skills.

会社説明