

シンガポールの求人なら JAC Recruitment Singapore

PR/096124 | Lead Signal Entegrity Engineer

募集職種

人材紹介会社

ジェイ エイ シー リクルートメント シンガポール

求人ID

1562506

業種

化学・素材

雇用形態

正社員

勤務地

台湾

給与

経験考慮の上、応相談

更新日

2025年11月04日 10:02

応募必要条件

キャリアレベル

中途経験者レベル

英語レベル

無し

日本語レベル

無し

最終学歴

短大卒: 準学士号

現在のビザ

日本での就労許可は必要ありません

募集要項

Company and Job Overview

The Lead Signal Integrity Engineer is a technical leader responsible for advancing laminate materials to meet and exceed high-speed electrical and signal integrity (SI) performance requirements. This role provides mentorship and guidance to the Signal Integrity team in Taiwan, drives innovation in SI testing methodologies, and ensures strong technical engagement with global OEMs. The Lead serves as a recognized authority in SI, aligning customer needs with material performance and representing the company in the high-performance electronics community.

Responsibilities

Customer-Facing Technical Support:

Lead technical engagement with OEMs and direct customers on high-speed laminate characterization.

Act as primary technical contact for SI-related design validation and adoption cycles.

Oversee the creation of technical reports, white papers, and collateral for internal and external use.

Strategic & Technical Leadership:

Define and develop advanced SI measurement, modeling, and simulation methodologies.

Collaborate with Product Management, R&D, and Sales to ensure alignment of SI capabilities with product strategy.

Represent company as a thought leader through publications, conferences, and industry forums.

Organizational Management:

Mentor, guide, and grow the Taiwan-based Signal Integrity Engineering team.

Establish scalable, cost-effective SI test methods that accelerate R&D and customer response.

Drive alignment with global Application Engineering teams to ensure best-in-class technical service.

Technology & Standards Thought Leadership:

Maintain expertise in SI methods, PCB processing effects, and high-speed digital design requirements.

Contribute to industry standards development and support customer forums on SI requirements. Top of Form

Qualifications

8+ years of experience in signal integrity engineering, PCB laminates, or high-speed design.

Expertise in VNA measurements, probing techniques, and advanced SI methodologies.

Experience with PCB manufacturing and processing effects on SI performance.

Demonstrated leadership and mentoring experience.

Proven record of technical publications, white papers, or conference presentations.

PhD or Master's in Electrical Engineering or related field required.

Fluent in English – required for global communication and technical documentation.

Proficiency in Mandarin Chinese – strongly preferred for engagement with Taiwan/China teams and customers.

Ability to travel regionally and globally as needed.

Catherine Qu JAC Recruitment Pte Ltd EA Personnel: R22104823 EA Personnel Name: QU QIUSHI

#LI-JACSG #countrysingapore

Notice: By submitting an application for this position, you acknowledge and consent to the disclosure of your personal information to the Privacy Policy and Terms and Conditions, for the purpose of recruitment and candidate evaluation.

Privacy Policy Link: https://www.jac-recruitment.sg/privacy-policy Terms and Conditions Link: https://www.jac-recruitment.sg/terms-of-use

会社説明