CareerCross by JAC Recruitment

PR/158619 | Digital IC Design Backend Manager

募集職種

人材紹介会社
ジェイ エイ シー リクルートメント マレーシア

求人ID
1540857

業種
その他（メーカー）

雇用形態
正社員

勤務地
マレーシア

給与
経験考慮の上、応相談

更新日
2025年06月03日 21:00

応募必要条件

職務経験
3年以上

キャリアレベル
中途経験者レベル

英語レベル
ビジネス会話レベル

日本語レベル
ビジネス会話レベル

最終学歴
短大卒： 準学士号

現在のビザ
日本での就労許可は必要ありません

募集要項

Company and Job Overview
A rapidly growing IC design platform company specializing in IP, SOC, and ASIC design services is seeking a talented and experienced Digital Backend IC Design Manager. Become part of a team of highly skilled engineers and designers who provide exceptional support to customers in High-Performance Computing, AI, 5G & Networking, and Automotive industries, utilizing cutting-edge technology.

Key Responsibilities
- Perform comprehensive digital backend tasks from netlist to GDS, at both the TOP and block levels, including Place and Route (PR), Static Timing Analysis (STA), Physical Verification (PV), Power Analysis (PA), and related activities.
- Collaborate closely with digital front-end engineers to troubleshoot and resolve issues such as timing discrepancies, SDC constraints, and UPF challenges.
- Execute block-level or Top-level Physical Design (PD) work of moderate to high complexity.
- Handle pre-mask and post-mask Engineering Change Orders (ECOs) efficiently.

Key Requirements
- Bachelor's degree or higher in Microelectronics or a related field, with over 7 years of relevant work experience.
- Comprehensive knowledge and experience in the complete design process, from Netlist to GDS.
- Proficient in one or more design tools, such as Innovus/ICC2, PT/Computers, LEC/Form, StarRC/QRC, PTPX/Volt, Caliber, etc.

- Preferred experience in successfully completing chip tape-outs with process sizes below 14nm, especially low-power design chips.
- Strong expertise in Top-level Place and Route (P&R) work, including tasks such as top-level partitioning, bump assignment, RDL routing, ESD planning, feedthrough insertion, and pin assignment.
- Priority consideration for candidates with proven Top-level Static Timing Analysis (STA) experience.
- Experience in Place and Route (P&R) for high-speed interfaces such as PCIE and DDR is highly desirable.

Benefit

- Competitive annual remuneration package complemented by attractive allowances
- Dynamic team composed of a vibrant workforce.
- Transparent and open work environment fostering collaboration and trust.

会社説明