



## PR/095109 | Principal Engineer

### 募集職種

### 人材紹介会社

ジェイ エイ シー リクルートメント シンガポール

### 求人ID

1540476

### 業種

その他 (メーカー)

### 雇用形態

正社員

### 勤務地

台湾

### 給与

経験考慮の上、応相談

### 更新日

2025年05月20日 12:18

## 応募必要条件

# 職務経験

3年以上

# キャリアレベル

中途経験者レベル

# 英語レベル

ビジネス会話レベル

# 日本語レベル

ビジネス会話レベル

# 最終学歴

短大卒: 準学士号

### 現在のビザ

日本での就労許可は必要ありません

### 募集要項

A reputed semiconductor equipment company is looking for an experienced Design Engineer to help them develop the Cadence SKILL tool.

## Responsibilities

Develop Automations using Cadence SKILLs to improve MLO/MLC design process.

Improve overall cycle from design to manufacturing through involvement in inter or intra departmental projects

Work with EDA vendors on new tools or new features evaluation

Perform multi-layer ceramic (MLC) and multi-layer organic (MLO) Design Engineering

## \* Secondary role

Work MLC/MLO physical layout (parts placement, routing, trace length adjustment, verification etc.) to understand the needs of MLO/MLC design work and improvement needed.

Design for manufacturability through working with MLC/MLO suppliers, apply best industry practices to reduce cost and maximize yield.

Develop design processes to reduce design cycle-time and defects and improve product performance.

<sup>\*</sup> Primary role

Support development projects

Requirements

Bachelor's Degree in Electrical Engineering. Diploma holders with at least 5 years of PCB design experience will be considered.

Experience in creating automation scripts using Cadence SKILLS is a must.

Proficiency in Cadence Allegro and Valor

MLC/MLO/PCB Design Experience with significant portion involving analog and mixed-signal design, and interfacing Fab houses to improve manufacturability.

Experience with designs utilizing blind, buried and micro vias would be advantageous.

Working knowledge in logical net-listings, schematics usage, electrical and routing rules creation, signal and power integrity optimization

Detail oriented, good team player and good track record of consistently meets committed project deadlines

Good communicator, written and verbal, using English

Good computer proficiency (MS Excel)

RF, back plane, electrical package design/routing experiences, related experience in a semiconductor testing environment, ATE industry will be advantageous.

Catherine Qu JAC Recruitment Pte Ltd EA Personnel: R22104823 EA Personnel Name: QU QIUSHI

会社説明