CareerCross by JAC Recruitment

PR/158519 | Senior / Staff / Principal Hardware Digital Engineer

募集職種

人材紹介会社
ジェイ エイ シー リクルートメント マレーシア

求人ID
1536569

業種
その他（メーカー）

雇用形態
正社員

勤務地
マレーシア

給与
経験考慮の上、応相談

更新日
2025年04月30日 16:02

応募必要条件

職務経験
3年以上

キャリアレベル
中途経験者レベル

英語レベル
ビジネス会話レベル

日本語レベル
ビジネス会話レベル

最終学歴
短大卒： 準学士号

現在のビザ
日本での就労許可は必要ありません

募集要項

Company and Job Overview
A highly reputable multinational corporation specializing in test and measurement systems is seeking talented individuals with a strong innovative mindset to join its growing R&D team. This is an exceptional opportunity to channel your passion for innovation and technology while thriving in dynamic environments that actively foster and nurture creativity.

Key Responsibilities
- Develop hardware features based on requirements from product management, including FPGA and CPLD development.
- Conduct technology research and oversee product bring-up, validation, verification, and debugging to ensure successful product launches.
- Collaborate with board-level designers on circuit design, schematic capture, layout review, simulation, and signal integrity analysis.
- Research and propose effective alternative parts to replace EOL components, minimizing software and hardware topology changes.
- Implement and simulate designs using CAD and synthesis tools (e.g., Mentor Graphics), and verify and validate hardware re-designs while debugging arising issues.
- Perform failure analysis to determine root causes during early validation and manufacturing builds, utilizing RCA techniques like fishbone diagrams.

- Incorporate Design for Manufacturing (DFM) inputs to enhance product yield and quality, and create mock-up designs as POCs to strengthen redesign proposals.
- Document failures and project progress, sharing both short- and long-term solutions with stakeholders.
- Mentor junior engineers, providing technical expertise and guidance, while leading the development of product and design documentation.
- Develop debugging tools and training materials for manufacturing teams during product release.

Key Requirements

- Bachelor’s or Master’s degree in Electrical/Electronic Engineering or Computer Engineering.
- Minimum 2 years of work experience in analog/digital design with expertise in board-level design or VHDL/SystemVerilog. For Principal Level, 8+ years of VHDL/Verilog/SystemVerilog experience; for Senior Level, 5+ years of experience.
- Strong expertise in HDL IP design or board-level digital circuit design, with proficiency in VHDL, Verilog, and SystemVerilog development, including FPGA design. Experience in testbench development is a plus.
- Knowledge of routing constraints for high-speed interfaces, circuit design with CPU/SoC/Micro-controllers, and use of hardware lab equipment (e.g., scopes, logic analyzers, signal generators, power supplies).
- Expertise in scripting/programming languages for test automation.
- Additional Strengths: Passionate about continuous learning in analog, digital, and computer technologies, with a strong work ethic and drive to succeed. R&D experience in HDL development for product or IP design is highly desirable.

会社説明