

PR/097823 | 2.5D / 3D Assembly Engineer

Job Information

Recruiter
JAC Recruitment Singapore

Job ID
1621110

Industry
Electronics, Semiconductor

Job Type
Permanent Full-time

Location
Singapore

Salary
Negotiable, based on experience

Refreshed
November 3rd, 2026 10:43

General Requirements

Minimum Experience Level
Over 6 years

Career Level
Mid Career

Minimum English Level
Native Level

Minimum Japanese Level
None

Minimum Education Level
Associate Degree/Diploma

Visa Status
No permission to work in Japan required

Job Description

2.5D / 3D Assembly EngineerAbout the Role
We are seeking a highly skilled **2.5D / 3D Assembly Engineer** to support the development and implementation of advanced semiconductor packaging and integration technologies. This role will focus on wafer-level packaging, 2.5D/3D assembly processes, package design optimization, reliability engineering, and advanced technology development.

The successful candidate will play a key role in driving innovation, improving assembly methodologies, collaborating with external partners, and developing next-generation packaging solutions for advanced semiconductor applications.

Key Responsibilities

- Lead the development and optimization of advanced semiconductor packaging and assembly technologies, including 2.5D and 3D integration.
- Support package design, assembly process development, and Design for Manufacturing (DFM) and Design for Test (DFT) initiatives.
- Perform thermo-mechanical, electrical, and reliability analysis using simulation and modeling tools.

- Investigate and resolve packaging, assembly, and reliability challenges across various operating environments.
- Collaborate with cross-functional teams, suppliers, and manufacturing partners to drive technology development and process improvements.
- Conduct failure analysis, root-cause investigations, and reliability assessments to improve product performance.
- Support the introduction of new materials, packaging technologies, and assembly methodologies.
- Contribute to technical documentation, design guidelines, and continuous improvement initiatives.

Requirements

- Master's or PhD in Mechanical Engineering, Materials Science, Physics, Semiconductor Packaging, Micro/Nanofabrication, or a related discipline.
- Strong hands-on experience in semiconductor assembly, packaging, or advanced integration technologies.
- Experience with wafer-level packaging, 2.5D/3D packaging, and advanced assembly processes.
- Knowledge of semiconductor package structures, materials, manufacturing processes, and reliability considerations.
- Familiarity with CAD tools and thermo-mechanical simulation methodologies.
- Experience with Finite Element Modeling (FEM) for thermal, mechanical, or electrical analysis.
- Strong understanding of assembly-related failure mechanisms and reliability engineering.
- Excellent analytical, troubleshooting, and engineering problem-solving skills.
- Solid understanding of material properties, physics fundamentals, and package behavior across varying environmental conditions.

Preferred Qualifications

- Experience developing Process Design Kits (PDKs) or packaging design flows.
- Knowledge of Through-Silicon Via (TSV), silicon processing, and thin-film technologies.
- Experience with cryogenic testing or low-temperature electro-mechanical characterization.
- Exposure to high-voltage or power semiconductor packaging qualification.
- Background in process engineering, manufacturing engineering, or advanced packaging development.

Notice: By submitting an application for this position, you acknowledge and consent to the disclosure of your personal information to the Privacy Policy and Terms and Conditions, for the purpose of recruitment and candidate evaluation.

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Company Description