

Design Verification Engineer

Job Information

Recruiter
JAC International Co., Ltd.

Hiring Company
Pioneering Edge AI and Next-Generation Semiconductor Innovation

Job ID
1619581

Industry
Other

Job Type
Permanent Full-time

Location
Tokyo - 23 Wards

Salary
8 million yen ~ Negotiable, based on experience

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General Requirements

Minimum Experience Level
Over 3 years

Career Level
Mid Career

Minimum English Level
Business Level

Minimum Japanese Level
Business Level

Minimum Education Level
Bachelor's Degree

Visa Status
Permission to work in Japan required

Job Description

As a Design Verification Engineer, you will play a key role in verifying next-generation AI accelerator SoCs and IPs used in cutting-edge edge AI solutions.

Working closely with architecture, design, and hardware engineering teams, you will develop advanced verification environments, improve verification methodologies, and ensure the quality and reliability of innovative semiconductor products.

■Key Responsibilities
-Develop and maintain verification environments for AI accelerator IP and SoC designs.
-Create and enhance SystemVerilog/UVM testbenches and verification infrastructure.
-Develop assertions, functional coverage, and verification methodologies.
-Perform RTL, gate-level, and SoC-level verification activities.
-Analyze coverage metrics and drive verification closure.
-Support power-aware verification and ASIC power analysis activities.
-Automate verification flows, reporting, and regression environments.

-Collaborate with design and architecture teams to resolve technical issues.

Employee Benefits:
-Competitive compensation package
-Performance-based bonus program
-Annual salary review
-Permanent employment
-Full remote work available
-Comprehensive social insurance coverage
-Opportunity to work on cutting-edge AI processor and semiconductor technologies
-International and collaborative working environment
-Professional development and continuous learning opportunities
-Career growth opportunities within a fast-growing deep-tech organization
-Exposure to advanced AI, semiconductor, and edge computing projects
-Smoke-free workplace
-Overtime typically ranging from approximately 0?20 hours per month

Required Skills

-6-7 years of experience in functional verification using SystemVerilog and UVM.
-Strong knowledge of verification methodologies, including coverage-driven and metric-driven verification.
-Experience developing verification environments from scratch.
-Experience verifying designs utilizing high-speed interfaces such as AXI4.
-Experience with gate-level simulation and timing/delay modeling.
-Experience with constraint-random verification methodologies.
-Experience developing functional coverage and performing code coverage analysis.
-Strong debugging skills for RTL and verification environments.
-Experience writing and debugging SystemVerilog assertions.
-Excellent communication and collaboration skills.

Company Description

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