

Accelerator IP Design Engineer (ASIC, RTL)

Job Information

Recruiter
JAC International Co., Ltd.

Hiring Company
Pioneering Edge AI and Next-Generation Semiconductor Innovation

Job ID
1619580

Industry
Other

Job Type
Permanent Full-time

Location
Tokyo - 23 Wards

Salary
8 million yen ~ Negotiable, based on experience

Refreshed
October 29th, 2026 17:13

General Requirements

Minimum Experience Level
Over 3 years

Career Level
Mid Career

Minimum English Level
Business Level

Minimum Japanese Level
Business Level

Minimum Education Level
Bachelor's Degree

Visa Status
Permission to work in Japan required

Job Description

As an Accelerator IP Design Engineer (ASIC, RTL), you will contribute to the design and development of next-generation AI accelerator IP and SoC solutions for edge AI applications.

Working closely with architecture, compiler, and verification teams, you will be responsible for RTL design, microarchitecture optimization, ASIC implementation activities, and system integration, helping to deliver highly efficient AI hardware platforms.

■Key Responsibilities
-Design and develop RTL modules for AI accelerator IPs.
-Perform module-level verification and debugging activities.
-Support synthesis, static timing analysis (STA), and power estimation.
-Optimize microarchitecture for performance, area, and power efficiency.
-Collaborate with architecture and compiler teams on new feature development.
-Support SoC integration activities using internal and third-party IPs.
-Participate in IP-level and SoC-level verification using SystemVerilog and UVM.
-Contribute to engineering best practices, documentation, testing, and CI workflows.

Employee Benefits:
-Bachelor's degree in Electrical Engineering, Computer Engineering, Computer Science, or a related discipline.
-Strong experience in RTL design and ASIC development.
-Experience with Verilog/SystemVerilog-based hardware design.
-Knowledge of synthesis, timing closure, and power optimization methodologies.
-Experience with digital design debugging and verification.
-Understanding of SoC architectures and IP integration.
-Strong problem-solving and analytical skills.
-Ability to collaborate effectively in a multidisciplinary engineering environment.

Required Skills

-Bachelor's degree in Electrical Engineering, Computer Engineering, Computer Science, or a related discipline.
-Strong experience in RTL design and ASIC development.
-Experience with Verilog/SystemVerilog-based hardware design.
-Knowledge of synthesis, timing closure, and power optimization methodologies.
-Experience with digital design debugging and verification.
-Understanding of SoC architectures and IP integration.
-Strong problem-solving and analytical skills.
-Ability to collaborate effectively in a multidisciplinary engineering environment.

Company Description

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