Bilingual Semiconductor Technical Lead

Job Information

Recruiter
Izumi Network Yugen Kaisha

Job ID
1615943

Industry
Electronics, Semiconductor

Job Type
Permanent Full-time

Location
Tokyo - 23 Wards

Salary
9 million yen ~ 16 million yen

Refreshed
November 2nd, 2026 07:00

General Requirements

Minimum Experience Level
Over 6 years

Career Level
Mid Career

Minimum English Level
Business Level

Minimum Japanese Level
Business Level

Minimum Education Level
Bachelor's Degree

Visa Status
Permission to work in Japan required

Job Description

Position Summary
We are seeking an experienced **Bilingual Semiconductor Technical Lead** to support advanced SoC implementation projects for Synopsys Japan.

The successful candidate will act as the onsite technical lead, working directly with customers in Japan while coordinating global engineering teams. This position requires strong expertise across the RTL-to-GDSII implementation flow, with particular focus on synthesis, timing closure, signoff, and tapeout activities.
This role combines technical leadership, customer engagement, and project execution responsibilities.

Key Responsibilities

- Act as the primary technical lead for customer-facing projects.
- Lead technical discussions with customers and internal engineering teams.
- Coordinate onsite and offshore engineering resources.
- Drive RTL-to-GDSII implementation activities.
- Support synthesis, timing closure, signoff, and tapeout execution.
- Drive Performance, Power, and Area (PPA) optimization.
- Identify technical risks and implementation bottlenecks.
- Collaborate closely with RTL, Physical Design, DFT, Verification, and EDA teams.
- Track project milestones and support successful project delivery.

Required Skills

Required Skills & Experience

- 8+ years of semiconductor design and implementation experience.
- Strong understanding of the complete RTL-to-GDSII implementation flow.

Hands-on experience in:

- Synthesis
- Static Timing Analysis (STA)
- Timing Closure
- Signoff Methodology
- Tapeout Activities

Experience with:

- Design Compiler
- Fusion Compiler
- PrimeTime
- SDC Constraint Development
- Logic Equivalence Check (LEC)

Strong understanding of how RTL decisions impact:

- Timing
- Power
- Congestion
- Testability
- Physical Implementation

1. Experience leading technical teams or project delivery activities.
2. Customer-facing experience is highly preferred.

Preferred Skills

- ICC2
- StarRC
- VC SpyGlass
- Floorplanning
- Place & Route (PnR)
- Clock Tree Synthesis (CTS)
- DRC/LVS
- Low Power Design
- Advanced-node implementation experience

Language Requirements:
Japanese: Business Level or above (**Mandatory**)
English: Business Level (**Mandatory**)

Preferred Background:
Candidates from the following companies or similar environments are highly preferred:

- Synopsys
- Cadence
- Socionext
- Renesas
- TSMC
- Rapidus Ecosystem
- Semiconductor Design Service Companies
- ASIC Design Houses

Company Description