



PR/160721 | IP Design Engineer (RTL & Synthesis | FPGA & High-Speed Interfaces)

Job Information

Recruiter

JAC Recruitment Malaysia

Job ID

1599405

Industry

Electronics, Semiconductor

Job Type

Permanent Full-time

Location

Malaysia

Salary

Negotiable, based on experience

Refreshed

June 26th, 2026 11:15

General Requirements

Minimum Experience Level

Over 6 years

Career Level

Mid Career

Minimum English Level

Fluent

Minimum Japanese Level

None

Minimum Education Level

Associate Degree/Diploma

Visa Status

No permission to work in Japan required

Job Description

Join a fast-growing semiconductor design organization developing cutting-edge FPGA IP solutions for next-generation networking and high-performance systems.

This role offers the opportunity to work across the full IP development lifecycle—from architecture definition to RTL implementation and silicon validation—while collaborating with global engineering teams. If you enjoy building scalable, high-performance designs and working on advanced protocols, this is a strong platform for career growth.

Key Responsibilities

- Understand FPGA architectures, application use cases, and protocol standards
- Define system architecture and develop algorithm models using C/C++ or MATLAB
- Develop high-quality RTL code using Verilog/VHDL
- Build verification environments using SystemVerilog

- Perform simulation, debugging, and validation to ensure design robustness
- Deliver complete IP solutions from concept to implementation
Package IP using EDA tools and develop user-friendly interfaces (GUI)
- Ensure IP quality through comprehensive testing and validation
- Provide technical training and guidance to FAEs
- Support customer integration, debugging, and deployment activities
- Gather feedback from field teams and customers to enhance IP performance and features
- Contribute to ongoing improvements and next-generation IP development

Key Requirements

- 5+ years of experience in FPGA / RTL / digital design
- Bachelor's degree or above in Electronics, Microelectronics, Communications, or Computer Science
- Strong proficiency in Verilog/VHDL
- Hands-on experience with FPGA tools: Vivado, ISE, or Quartus
- Experience with simulation tools: Synopsys VCS, Verdi, Cadence, or ModelSim
- Solid understanding of digital front-end design and timing closure
- Knowledge of FPGA development methodologies (top-down / bottom-up)
- Familiarity with DFT concepts and performance optimization
- Strong problem-solving mindset with innovative thinking
- Good communication skills and ability to collaborate across teams
- Ability to manage tasks and contribute in a fast-paced environment

Nice-to-Have (Stand Out Skills)

- DSP / Algorithm Design
- Experience with FIR, FFT, DUC/DDC, CFR
- Familiarity with Xilinx System Generator
- High-Speed Interfaces
- Experience with protocols such as PCIe, NVMe, SATA, SRIO, or AURORA

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Company Description