



【800～2500万円】Digital Design Engineer

外資系半導体メーカーでの募集です。弱電回路設計のご経験のある方は歓迎です。

Job Information

Recruiter

JAC Recruitment Co., Ltd.

Hiring Company

外資系半導体メーカー

Job ID

1593778

Industry

Electronics, Semiconductor

Company Type

International Company

Job Type

Permanent Full-time

Location

Tokyo - 23 Wards

Salary

8 million yen ~ 25 million yen

Work Hours

09:00 ~ 18:00

Holidays

詳細は求人ご紹介時にご案内いたします。

Refreshed

June 25th, 2026 06:00

General Requirements

Career Level

Mid Career

Minimum English Level

Business Level

Minimum Japanese Level

Native

Minimum Education Level

Bachelor's Degree

Visa Status

Permission to work in Japan required

Job Description

【求人No NJB2381570】

- ・ Developing micro architecture specification of the logic circuit from reading and comprehending the Product Requirement Document (PRD) .
- ・ Developing the Register Transfer Level (RTL) design from the micro architecture specification using Verilog or SystemVerilog as the HDL.
- ・ Developing standalone test benches to verify the RTL behavior.
- ・ Writing and verifying SystemVerilog Assertions (SVA) for a design.

- Writing timing constraints and clock definition for synthesis and place and route tools.
 - Running industry standard synthesis tools (e.g. Genus or Design Compiler) and being able to fix timing problems if they arise.
 - Understanding various design tradeoffs including timing/area/power and knowing how to improve them.
 - Reading and understanding the Static Timing Analysis (STA) reports from an industry standard STA tool (e.g. Prime Time) .
 - Cross functional interactions and communication with various teams within SiTime including analog verification backend system and test engineering teams.
 - Post Si bring up validation and debugging.
-

Required Skills

【Qualifications Requirements】

- Master's degree in electrical engineering plus 5 years of relevant work experience in the industry.
- Excellent verbal and written communication skills in English.
- Proficient in Verilog and SystemVerilog.
- Expertise in digital logic design fundamentals such as clock divider circuits multi clock logic designs CDC FIFO FSM etc.
- Experience in designing mixed signal digital logic.
- Basic understanding of Discrete time Signal Processing theory FIR and IIR filter design.
- Solid experience in digital design flow including RTL design synthesis timing constraints and STA.
- Skilled in scripting languages Perl/Tcl/Python.

【Desired Characteristics Attributes】

- Ph.D. in electrical/computer engineering plus 3 years of relevant industry experience.
 - 2 5 years of experience in designing high precision digital arithmetic logic and Digital Signal Processing.
 - 2 5 years of experience in designing Digital Phase Locked Loops (DPLL) .
 - Experience in complex FSM design.
 - Familiarity with MATLAB Simulink or any other high level modeling tools.
 - Experience in low power digital design flow.
 - Basic understanding of the Control Theory.
-

Company Description

ご紹介時にご案内いたします