【800 ~ 2500万円】Verification Engineer

外資系半導体メーカーでの募集です。 弱電回路設計のご経験のある方は歓迎です。

Job Information

Recruiter
JAC Recruitment Co., Ltd.

Hiring Company
外資系半導体メーカー

Job ID
1593777

Industry
Electronics, Semiconductor

Company Type
International Company

Job Type
Permanent Full-time

Location
Tokyo - 23 Wards

Salary
8 million yen ~ 25 million yen

Work Hours
09:00 ~ 18:00

Holidays
詳細は求人ご紹介時にご案内いたします。

Refreshed
June 25th, 2026 06:00

General Requirements

Career Level
Mid Career

Minimum English Level
Business Level

Minimum Japanese Level
Native

Minimum Education Level
Bachelor's Degree

Visa Status
Permission to work in Japan required

Job Description

【求人No NJB2381564】
・Developing SV RNM models for both analog and mixed signal circuits
・Developing verification plan from chip or block specifications
・Developing UVM based verification environment（scoreboards monitors sequencers etc.）
・Developing digital top verification in System Verilog
・Defining and writing System Verilog Assertions（SVA）
・Defining and writing functional coverages and covergroups

・Running simulations and debugging simulation results
・Reviewing verification results for Tape out sign off
・Communicating with stakeholders（design/test/verification）to facilitate teamwork and efficient sharing of information and exchange of ideas

Required Skills

【Qualifications Requirements】
・MS（BS）degree in electrical/computer engineering or related fields with 5（8）years of work experience doing verification in the semiconductor industry
・Good verbal and written communication skills in English
・Proficient in SystemVerilog and SystemVerilog OOP
・Fluency in utilizing scripting languages such as Perl / Python
・Proficient（through work experience）in verification using UVM
・Strong experience writing SystemVerilog Assertions（SVA）
・Understanding of Analog schematic and experience with Cadence Virtuoso
・Basic understanding of digital design using Verilog
・Ability to communicate and work effectively with geographically dispersed teams of mixed signal digital design and analog design engineers
・Ability to work independently and drive solutions to challenging problems

【Desired Qualification】
・Experience with generating functional models for analog blocks using SystemVerilog RNM Wreal（V AMS）or similar techniques
・Experience with UVM AMS methodology
・Solid experience with Formal Property Verification（FPV）
・Programming experience writing OOP code in C++
・Excellent written and verbal communication skills in English
・Experience with performing analog mixed signal verification
・Proven track record in working well with others in fast paced and collaborative work environment
・Knowledge of analog design
・Knowledge of synthesizable digital design
・Experience working on verification of datapath designs including filters

Company Description

ご紹介時にご案内いたします