

【800 ~ 2500万円】Analog Mixed Signal Design Engineer

外資系半導体メーカーでの募集です。 弱電回路設計のご経験のある方は歓迎です。

Job Information

Recruiter
JAC Recruitment Co., Ltd.

Hiring Company
外資系半導体メーカー

Job ID
1593774

Industry
Electronics, Semiconductor

Company Type
International Company

Job Type
Permanent Full-time

Location
Tokyo - 23 Wards

Salary
8 million yen ~ 25 million yen

Work Hours
09:00 ~ 18:00

Holidays
詳細は求人ご紹介時にご案内いたします。

Refreshed
November 13th, 2026 09:00

General Requirements

Career Level
Mid Career

Minimum English Level
Business Level

Minimum Japanese Level
Native Level

Minimum Education Level
Bachelor's Degree

Visa Status
Permission to work in Japan required

Job Description

【求人No NJB2381318】
・Contribute to the architectural definition of the design and chip integration
・Technical leader for chip level design and verification simulations to ensure building blocks meet specifications at the schematic level and after post layout extraction while fully provisioning for DFT and DFM
・Work closely with Layout Engineers to validate proper layout using all best known methods
・Document assigned blocks and hold preliminary and final design review meetings
・Actively participate in the chip bring up evaluation and characterization with emphasis on owned blocks

・Work cross functionally with Product Characterization Test and Application Engineers on issues related to owned circuit blocks
・Coach mentor and develop junior/mid level analog designers foster cross functional collaboration.

Required Skills

【Qualifications Requirements】
・M.S. in Electrical Engineering or related field with minimum 15 years of related experience or Ph.D. in Electrical Engineering with minimum 12 years of related experience
・Excellent academic record with published research projects prototyped and proven in silicon
・Detailed knowledge of CMOS circuits and noise analysis
・Core expertise in one of the following areas:
  ・Integer N and fractional N PLL
  ・Sigma Delta ADCs
  ・Temperature sensor
  ・Analog and digital filters
  ・Quartz or MEMS oscillator
  ・Sub threshold circuits
  ・Low noise regulator and bandgap
  ・High speed output drivers
・Ability to oversee circuit layout for critical blocks
・Knowledge of programming languages: MATLAB VerilogA
・Proficient in using Cadence analog design tools
・Good facilitation skill for project/design review meeting
・Excellent analytical problem solving written/verbal communication.
・Proven leadership and ability to collaborate across system architects digital teams layout test manufacturing

【Desired Characteristics Attributes】
・Passionate self starter with a strong commitment to flawless execution
・Excellent written and verbal communication skills required
・Ability to work well with others in a fast paced collaborative team environment

Company Description

ご紹介時にご案内いたします