CareerCross by JAC Recruitment

PR/159403 | Chip Operation Product Engineer

Job Information

Recruiter
JAC Recruitment Malaysia

Job ID
1553827

Industry
Other (Manufacturing)

Job Type
Permanent Full-time

Location
Malaysia

Salary
Negotiable, based on experience

Refreshed
August 5th, 2025 10:20

General Requirements

Minimum Experience Level
Over 3 years

Career Level
Mid Career

Minimum English Level
Business Level

Minimum Japanese Level
Business Level

Minimum Education Level
Associate Degree/Diploma

Visa Status
No permission to work in Japan required

Job Description

Our client is the global leader in mining consulting and services. They offer complete design and manufacturing system of blockchain miners and are now looking for a Chip Operation Product Engineer to join their ever-growing team.

Job Responsibilities

- Collaborate with chip and packaging design teams to conduct DFM (Design for Manufacturability) check to ensure Si and package manufacturability.
- Work with product team to estimate the chip yield and set appropriate SKU combination binning scheme.
- Interface foundry on Si fabrication, take charge of Si wafer NTO planning, performing WAT and yield analysis. Drive foundry on corrective actions for yield loss or quality degradation.
- Interface OSAT on wafer bumping and assembly. Ensure bumping and substrate DFM inputs from OSAT be implemented into package design, and co-define process BKM with vendors and monitor process quality.
- Perform chip level and package reliability qual with collaboration with internal product team and suppliers. Ensure chip package meeting application spec.
- Working with ATE team on chip CP and FT test coverage and yield analysis. Monitor yield trend and identify failure mechanism by fast eFA and pFA. .

- Assist the quality department in analyzing customer RMAs and provide technical and experimental suggestions.

Job Requirements

- A bachelor's degree or above major in microelectronics, physics, or material science or electrical engineering.
- 3 years experience on Si chip product engineering, prefer on digital chips. Experienced on interface with foundry or package house.
- Understanding semiconductor fabrication and test flow. Knowledge of advanced CMOS, advanced package is a plus.
- Knowledge on common CMOS Si and package failure, mechanism, and corrective action is a plus.
- Knowledge on JEDEC reliability spec, qualification flow, and quality spec is a plus.
- Familiar with common failure analysis methods such as SEM, X-Ray, EMMI, and SAT is a plus.
- Skilled on statistical yield data analysis, and proficient on using YMS tools.

Notice: By submitting an application for this position, you acknowledge and consent to the disclosure of your personal information to the Privacy Policy and Terms and Conditions, for the purpose of recruitment and candidate evaluation.

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Company Description