



PR/158619 | Digital IC Design Backend Manager

Job Information

Recruiter
[JAC Recruitment Malaysia](#)
Job ID

1548058

Industry

Other (Manufacturing)

Job Type

Permanent Full-time

Location

Malaysia

Salary

Negotiable, based on experience

Refreshed

July 8th, 2025 16:31

General Requirements

Minimum Experience Level

Over 3 years

Career Level

Mid Career

Minimum English Level

Business Level

Minimum Japanese Level

Business Level

Minimum Education Level

Associate Degree/Diploma

Visa Status

No permission to work in Japan required

Job Description

Company and Job Overview

A rapidly growing IC design platform company specializing in IP, SOC, and ASIC design services is seeking a talented and experienced Digital Backend IC Design Manager. Become part of a team of highly skilled engineers and designers who provide exceptional support to customers in High-Performance Computing, AI, 5G & Networking, and Automotive industries, utilizing cutting-edge technology.

Key Responsibilities

- Perform comprehensive digital backend tasks from netlist to GDS, at both the TOP and block levels, including Place and Route (PR), Static Timing Analysis (STA), Physical Verification (PV), Power Analysis (PA), and related activities.
- Collaborate closely with digital front-end engineers to troubleshoot and resolve issues such as timing discrepancies, SDC constraints, and UPF challenges.
- Execute block-level or Top-level Physical Design (PD) work of moderate to high complexity.
- Handle pre-mask and post-mask Engineering Change Orders (ECOs) efficiently.

Key Requirements

- Bachelor's degree or higher in Microelectronics or a related field, with over 7 years of relevant work experience.
- Comprehensive knowledge and experience in the complete design process, from Netlist to GDS.
- Proficient in one or more design tools, such as Innovus/ICC2, PT/Computers, LEC/Form, StarRC/QRC, PTPX/Volt, Caliber, etc.

- Preferred experience in successfully completing chip tape-outs with process sizes below 14nm, especially low-power design chips.
- Strong expertise in Top-level Place and Route (P&R) work, including tasks such as top-level partitioning, bump assignment, RDL routing, ESD planning, feedthrough insertion, and pin assignment.
- Priority consideration for candidates with proven Top-level Static Timing Analysis (STA) experience.
- Experience in Place and Route (P&R) for high-speed interfaces such as PCIe and DDR is highly desirable.

Benefit

- Competitive annual remuneration package complemented by attractive allowances
- Dynamic team composed of a vibrant workforce.
- Transparent and open work environment fostering collaboration and trust.

Notice: By submitting an application for this position, you acknowledge and consent to the disclosure of your personal information to the Privacy Policy and Terms and Conditions, for the purpose of recruitment and candidate evaluation.

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Company Description