CareerCross by JAC Recruitment

PR/095186 | Substrate Engineer - Cadence SKILL

Job Information

Recruiter
JAC Recruitment Singapore

Job ID
1538322

Industry
Other (Manufacturing)

Job Type
Permanent Full-time

Location
Taiwan

Salary
Negotiable, based on experience

Refreshed
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General Requirements

Minimum Experience Level
Over 3 years

Career Level
Mid Career

Minimum English Level
Business Level

Minimum Japanese Level
Business Level

Minimum Education Level
Associate Degree/Diploma

Visa Status
No permission to work in Japan required

Job Description

Company and Job Overview

This is an well developed and ambitious semiconductor equipment company. They are looking for an experienced Substrate Engineer to be based in Hsinchu, Taiwan.

Responsibilities

* Primary role

Develop Automations using Cadence SKILLs to improve MLO/MLC design process.

Improve overall cycle from design to manufacturing through involvement in inter or intra departmental projects

Work with EDA vendors on new tools or new features evaluation

Perform multi-layer ceramic (MLC) and multi-layer organic (MLO) Design Engineering

* Secondary role

Work MLC/MLO physical layout (parts placement, routing, trace length adjustment, verification etc.) to understand the needs of MLO/MLC design work and improvement needed.

Design for manufacturability through working with MLC/MLO suppliers, apply best industry practices to reduce cost and maximize yield.

Develop design processes to reduce design cycle-time and defects and improve product performance.

Support development projects

Job Requirements

Bachelor’s Degree in Electrical Engineering. Diploma holders with at least 5 years of PCB design experience will be considered.

Experience in creating automation scripts using Cadence SKILLS is a must.

Proficiency in Cadence Allegro and Valor

MLC/MLO/PCB Design Experience with significant portion involving analog and mixed-signal design, and interfacing Fab houses to improve manufacturability.

Experience with designs utilizing blind, buried and micro vias would be advantageous.

Working knowledge in logical net-listings, schematics usage, electrical and routing rules creation, signal and power integrity optimization

Detail oriented, good team player and good track record of consistently meets committed project deadlines

Good communicator, written and verbal, using English

Good computer proficiency (MS Excel)

RF, back plane, electrical package design/routing experiences, related experience in a semiconductor testing environment, ATE industry will be advantageous.

Catherine Qu
JAC Recruitment Pte Ltd
EA Personnel: R22104823
EA Personnel Name: QU QIUSHI

#LI-JACSG
#countrysingapore

Company Description